REMARKS

Claims 1-4, 6-18, 20-23, and 25-36 are pending. By this Amendment, Claims 1, 4, 6, 7, 15, 18, 19, 23, 26 and 32 are amended, and Claims 5, 19 and 24 are canceled

The subject matter of Claims 5, 19 and 24 has been respectively incorporated into Claims 4, 18 and 23.

Applicants gratefully acknowledge the indication in the Office Action that Claim 36 contains allowable subject matter.

Claim Rejection – 35 U.S.C. §101

Claims 1-19 were rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter.

Applicants respectfully submit that Claims 1, 4, 6, 15 and 18 as amended obviate this rejection.

Claim Rejection – 35 U.S.C. §102

Claims 4, 5, 18, 19, and 23 were rejected under 35 U.S.C. §102(b) as being anticipated by Prabu (U.S. Patent No. 6,463,525). This rejection is respectfully traversed.

Prabu discloses that first and second single precision operands are copied from respective first and second rows of a re-order buffer into first and second portions of a fifth row of the re-order buffer, thereby concatenating the first and second single precision operands to represent a first double precision operand. A second merge instruction can perform similar functions, by copying third and fourth single precision operands from respective third and fourth rows of the re-order buffer into first and second portions of a sixth row of the re-order buffer, thereby concatenating the third and fourth single precision operands to represent a second, double precision operand. See, for example, Prabu at column 3, lines 25-43 (C3/L25-43).

Prabu's first and second rows of the re-order buffer are wholly different from the fifth row, and the third and fourth rows are wholly different from the sixth row of the re-order buffer. They are not aliased.

Accordingly, Prabu fails to disclose or suggest "*a first instruction to merge plural lesser width registers* ***aliased onto a first greater width source register*** *of the greater width consumer instruction, the plural lesser width registers to be merged into a first temporary register*" and "*a second instruction to merge plural lesser width registers* ***aliased onto a second greater width source register*** *of the greater width consumer instruction, the plural lesser width registers to be merged into a second temporary register*", as recited in Claim 4, and similar features recited in Claims 18 and 23. See, for example, Figure 4 and numbered paragraph [1035] of the present application, which are encompassed by Claims 4, 18 and 23.

Claim Rejection – 35 U.S.C. §103

Claims 1, 15, 17, and 20-22

Claims 1, 15, 17, and 20-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nair (U.S. Patent No. 6,195, 746). This rejection is respectfully traversed.

Nair states that a type specifier associated with a register specifier determines which execution unit a register specifier will be allocated to, see e.g. column 4, lines 1-6 (C4/L1-6). Nair further discloses that LOAD and CAST instructions (but not STORE instructions) can include a target type specifier field. When the LOAD or CAST instruction is executed, a type of the register indicated as the target in the LOAD or CAST instruction will be changed to match the type indicated in the target type specifier field of the LOAD or CAST instruction. See, for example, Nair at C5/L41-65 and C6/L8-10.

Thus, in Nair the LOAD or CAST instructions relabel a register to a different type, a type that is *consistent* with the execution unit that will consume it. In other words, Nair must change

the type of a source register specifier so that it *matches* a type of the execution unit that will consume it.

In contrast, exemplary embodiments of the present invention encompassed by independent Claims 1, 6, 15, 20, 25, 31 assign a register having a first type (e.g., a greater width register that will receive the output of a greater width producer instruction) as a source register for an instruction having a *different* type (e.g., a lesser width consumer instruction).

Accordingly, Nair fails to disclose or suggest "*the processor executing the greater width producer instruction and placing a result of the execution in the greater width source register; and the processor executing the lesser width consumer instruction using the greater width source register*", as recited in Claim 1, and similar features recited in independent Claims 1, 15 and 20.

Claims 2, 3, 6-10, 16, 23, and 25-35

Claims 2, 3, 6-10, 16, 23, and 25-35 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nair in view of Prabu.

This rejection is traversed.

In particular with respect to Claims 7, 26 and 32, Nair and Prabu fail to disclose or suggest "*stalling at least one instruction of a fetch group if a dependency exists between an instruction in the fetch group and both an active lesser width producer instruction and an active greater width producer instruction,* ***until*** *at least one of the active lesser width producer instruction or the active greater width producer instruction is retired, and then resuming execution*", as recited in Claim 7, and similar features recited in Claims 26 and 32. The Examiner cites Nair at C7/L2-17, but this merely discloses that a run-time exception is generated if conversion between types is not supported. Nair does not disclose or suggest what happens after the exception is generated, and certainly does not disclose or suggest the details recited in Claims 7, 26 and 32. Prabu fails to overcome this deficiency of Nair, and thus Nair and Prabu fail to disclose or suggest Claims 7, 26 and 32.

Applicants further note that Prabu fails to overcome the deficiencies of Nair with respect to independent Claims 1 and 15, and therefore dependent Claims 2-3 and 16 are likewise allowable for at least the same reasons. Independent Claims 6, 23, 25 and 31 are also allowable for at least the same reasons as independent Claims 1 and 15.

Claims 11-14

Claims 11-14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nair and Prabu, and in further view of Yeager (U.S. Patent No. 6,216,200).

Claims 11-14 depend from allowable Claim 6, and are therefore likewise allowable for at least the same reasons. Yeager fails to overcome the deficiencies of Nair and Prabu with respect to Claim 6 discussed above.

Claim 24

Claim 24 was rejected under 35 U.S.C. §103(a) as being unpatentable over Prabu in further view of Nair. Cancellation of Claim 24 obviates this rejection. Claim 23 (into which the subject matter of Claim 24 is amended) is discussed above.

Conclusion

Applicant respectfully submits that the application is in condition for allowance. Favorable consideration on the merits and prompt allowance are respectfully requested. In the event any questions arise regarding this communication or the application in general, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

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Respectfully submitted,

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